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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Schloesser, et al. Docket No.: INF-135
Serial No.: 10/777,128 Art Unit: 2818
Filed: February 13, 2004 Examiner: TBD
For: Method of Fabricating and Architecture for Vertical Transistor Cells and Transistor-Controlled Memory Cells

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Date of Deposit: August 11, 2004

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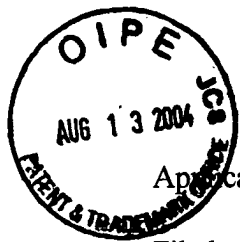
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Respectfully submitted,

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Dear Sir:

Applicants wish to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO/SB/08a that may be considered material to the examination of the above-identified application.

No fee is due at this time, as this Information Disclosure Statement is being filed pursuant to 37 C.F.R. § 1.97(b)(3), before the mailing of a first Office action on the merits.

Respectfully submitted,

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August 11, 2004

Date

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Substitute for form 1449A/PTO

(Use as many sheets as necessary)

Complete if Known

Application Number	10/777,128
Filing Date	2/13/2004
First Named Inventor	Schloesser, et al.
Art Unit	2818
Examiner Name	TBD
Attorney Docket Number	INF-135

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U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

**Examiner
Signature**

Date
Considered

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